Silicon Detector, Part I
VTX pixels, New strip tracker

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Outline

- Physics-driven detector requirements
- Intermediate tracker option
- Material effects to Y measurements
- Scenarios and funding requests
- R&D status
- Summary

Physics-driven detector requirements

1.Upsilon

1. Separation of $\Upsilon(1S)$, $\Upsilon(2S)$, and $\Upsilon(3S)$
2. Good mass resolution, namely good mom. resolution is required.
3. Goal is 100 MeV/c, but what resolution is really needed?

2.b-tag jet

1. DCA resolution ~ 100 μm at $p_T > 1$ GeV/c.
2. Tracking from vertex detector to outer tracker.

3.Jet structure

1. High priority: good efficiency for high-p_T track (> 1 GeV/c).
2. Low priority: low efficiency is acceptable for low-p_T track (< 1 GeV/c).

Physics-driven detector requirements

What’s are required for tracker?

1. ***For upsilon measurements,***
   - Large radius outer tracker is needed for momentum resolution.

2. ***For b-tag jet measurements,***
   - Pixel detector must be placed as close as beam pipe.
   - Tracking across pixel and outer tracker.
   - Momentum resolution as high as Upsilon measurements is not required. So large radius outer tracker is not necessary only for b-tag jet.

Thus, in order to meet the requirements 1 and 2 simultaneously, **we need intermediate tracker to link pixel and large radius outer tracker.**

Physics-driven detector requirements

So, what kind of intermediate tracker is required?

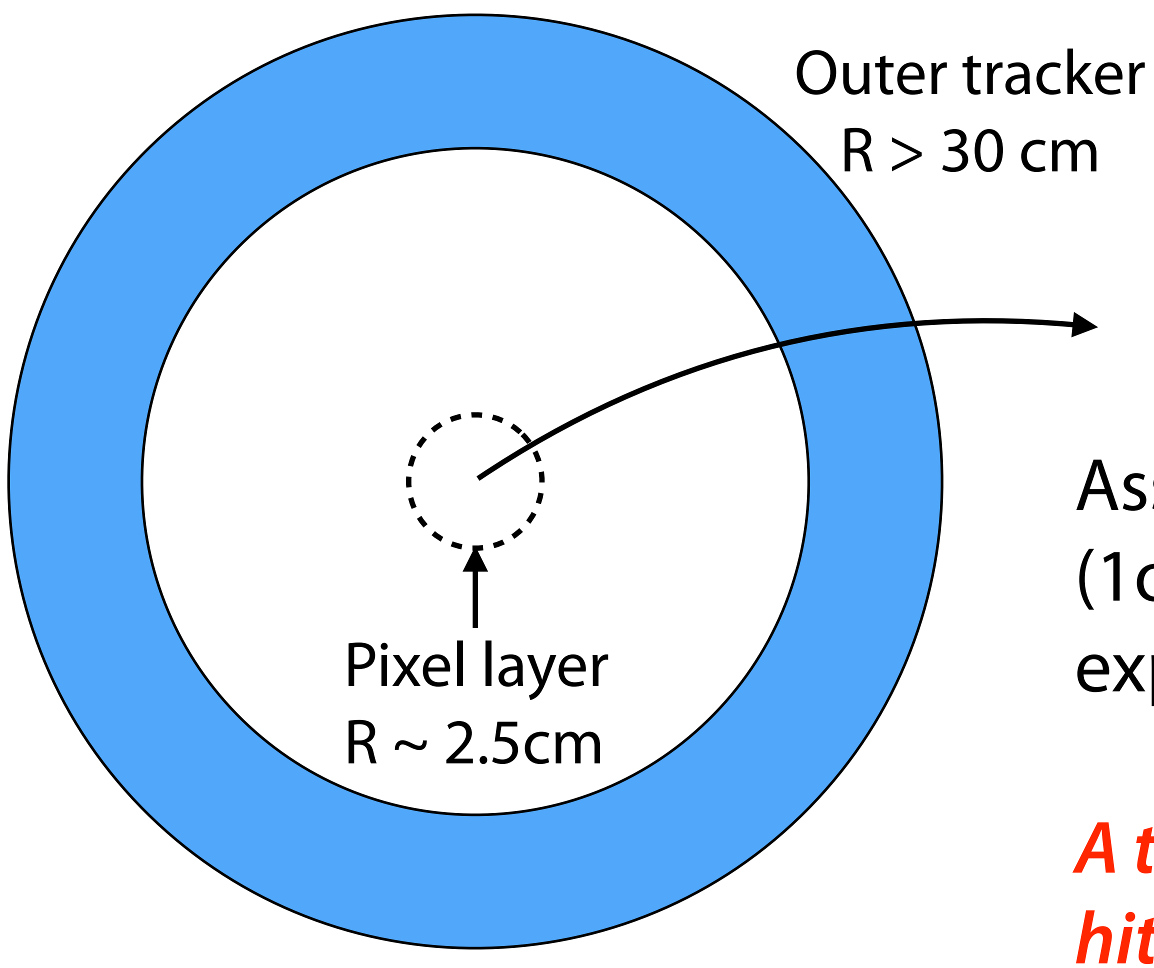
Necessary condition:

- 1 pixel layer only
  - outer tracker to pixel association does not work at all.
- 1 pixel layer + 1 more tracking layer nearby the pixel layer
  - remains many fake tracks.
- 1 pixel layer + 2 more tracking layers
  - least number of layers to determine the track momentum near the vertex.
  - enables unique association using the position and the momentum vector.
- **1 pixel layer + 3 more tracking layers**
  - **1 additional layer gives redundancy for robust tracking.**

Sufficient condition:

- requires MC simulations for estimating how many layers is needed for sufficiently small fake rate.

1 pixel layer only



Assuming the typical angular resolution (1σ) of outer tracker as 1 mrad, ~ 1 hit is expected in 5 mm^2 (3σ) at the pixel layer.

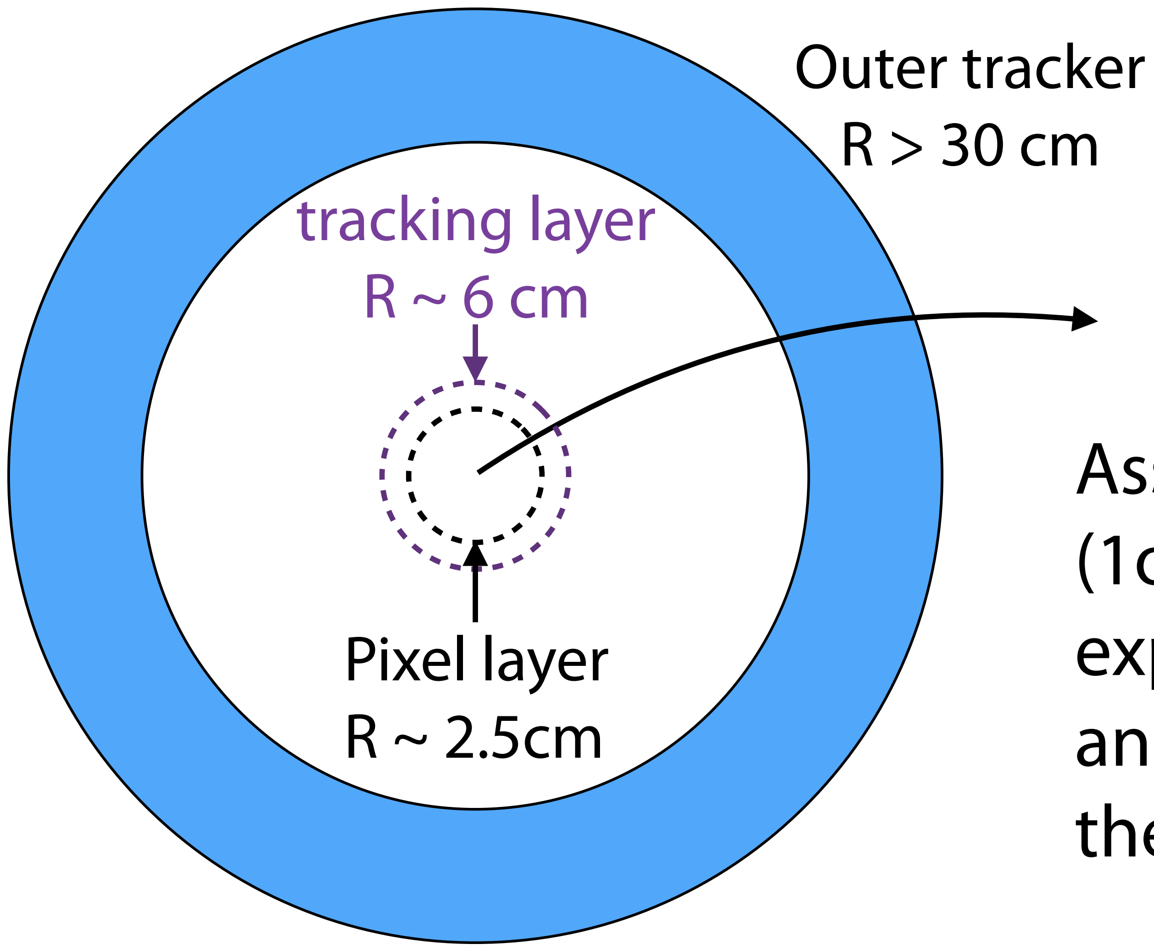
A track from outer tracker always gets fake hits at the pixel layer.

Position

~~Vector~~

~~Momenta~~

1 pixel layer + 1 more tracking layer

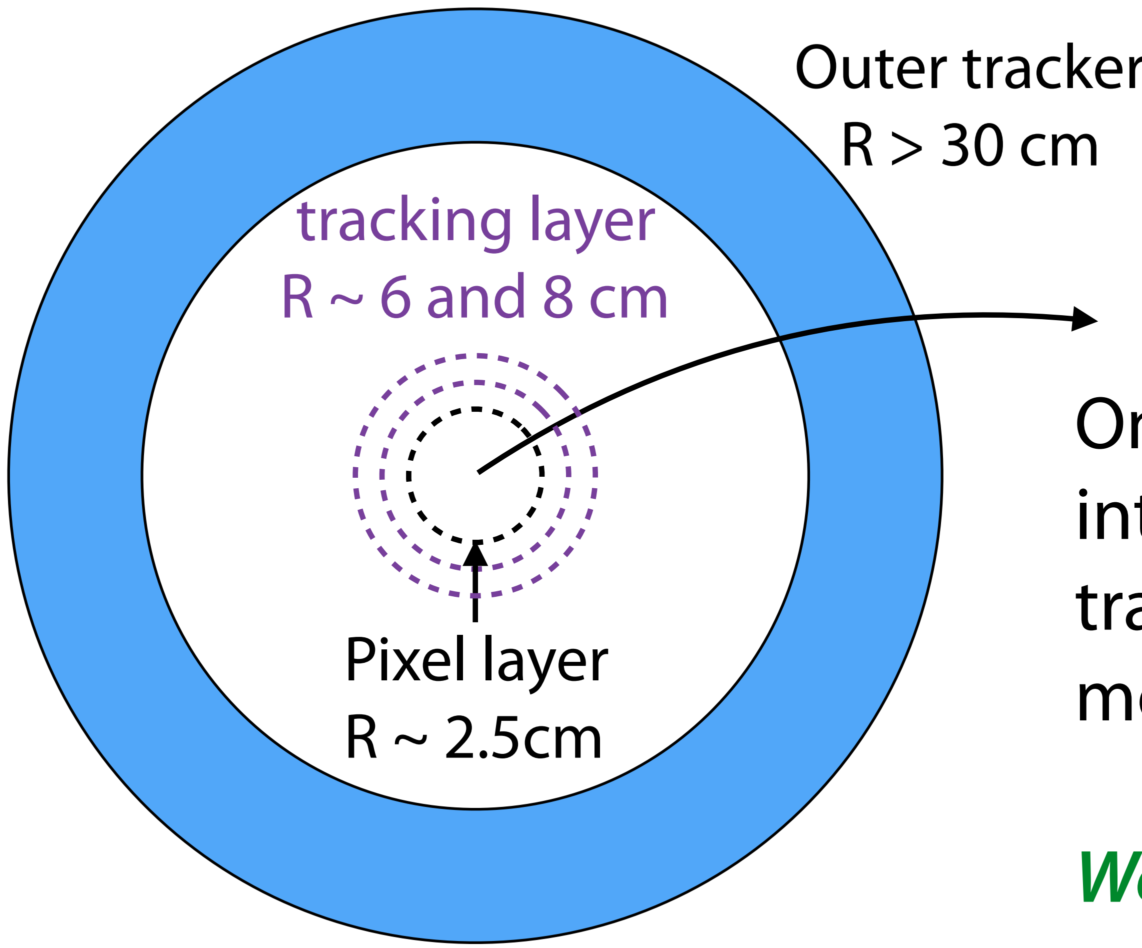


Assuming the typical angular resolution (1σ) of outer tracker as 1 mrad, ~ 1 hit is expected in 5 mm^2 (3σ) at the pixel layer and ~ 0.1 hit is expected in 4 mm^2 (3σ) at the tracking layer.

Position
Vector
~~Momenta~~

A track from outer tracker easily associates with fake tracks at the tracking layer.

1 pixel layer + 2 more tracking layers



Once we get three hits at the pixel and intermediate tracking layers along the track, we obtain position, direction, and momenta information.

We can reduce track candidates to be associated with a track from outer tracker.
1 more additional layer gives redundancy for robust tracking.

Position
Vector
Momenta

Cost consideration

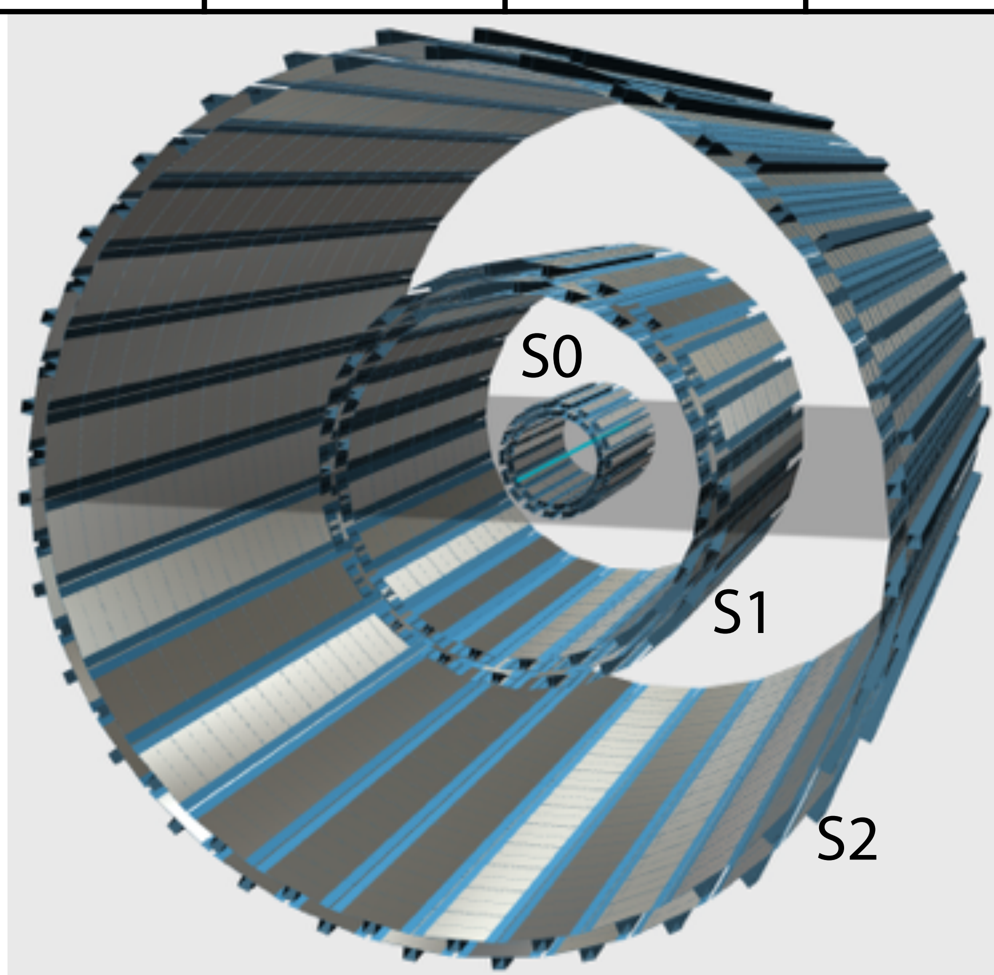
- Re-use of VTX pixel
  - is the lowest cost option of vertex detector.
  - should be standby in a case MAPS would not be available.
  - we have no reason to close this option now and thus have made an effort to maintain VTX pixel.

- Compact si-strip detector
  - is the most cost-effective way to realize such an intermediate tracker for achieving physics requirements.
  - si-strip itself is well know technology and we have already had experiences.
  - R&D and development of Geant4 simulations are ongoing.

Proposed design (VTXP/MAPS + Si-Strip)

Proposal in the pCDR

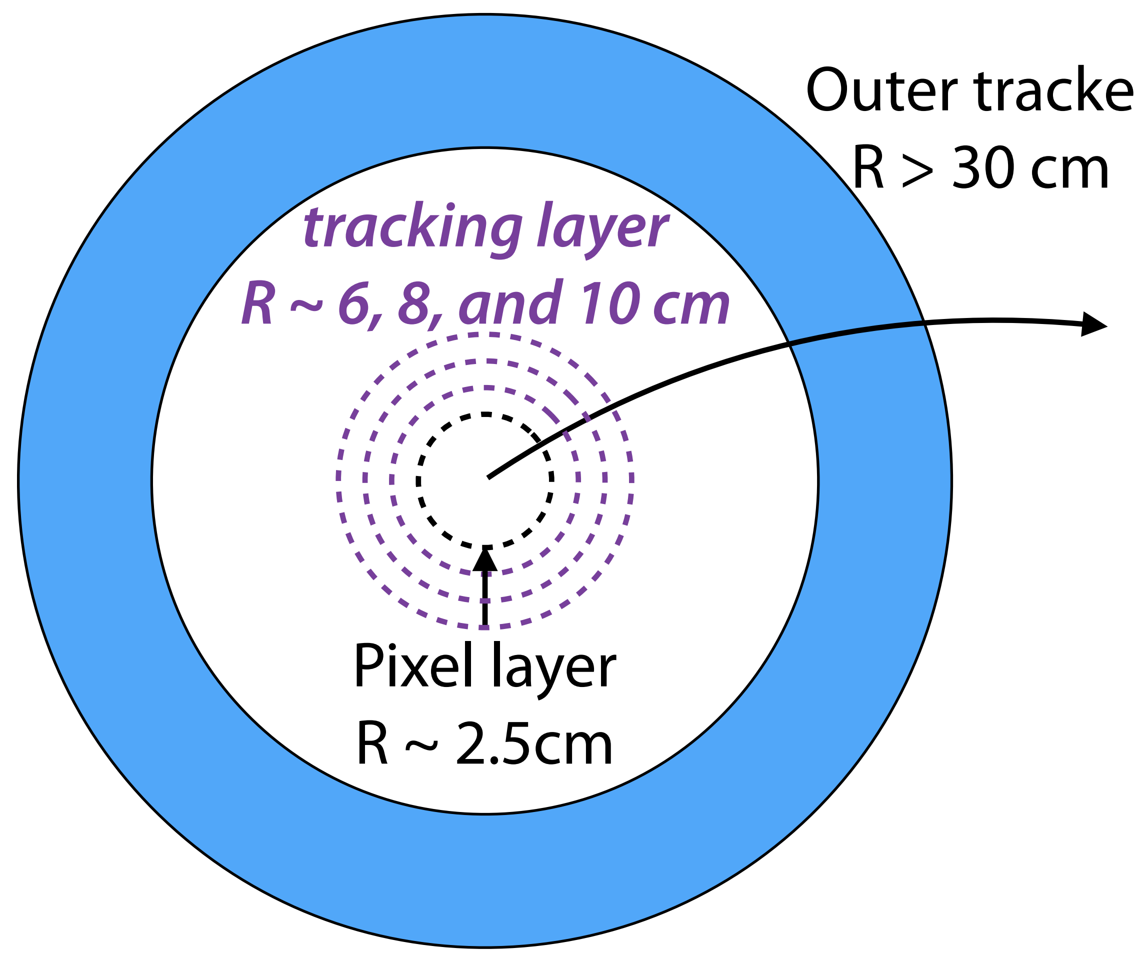
Layer	R (cm)	X0 (%)	Ganging
VTX Pixel	2.2, 4.4	1.3, 1.3	0
S0	7.7, 8.5	1.0, 1.0	0
S1	31, 34	0.6, 0.6	2
S2	64	1.0	5



More compact design

focuses on a track association of pixel to outer tracker

Layer	R (cm)	X0 (%)	Ganging
VTXP/MAPS	2.5	1.3	0
S0a	6	1.0	0
S0b	8	1.0	0
S0c	10	1.0	0

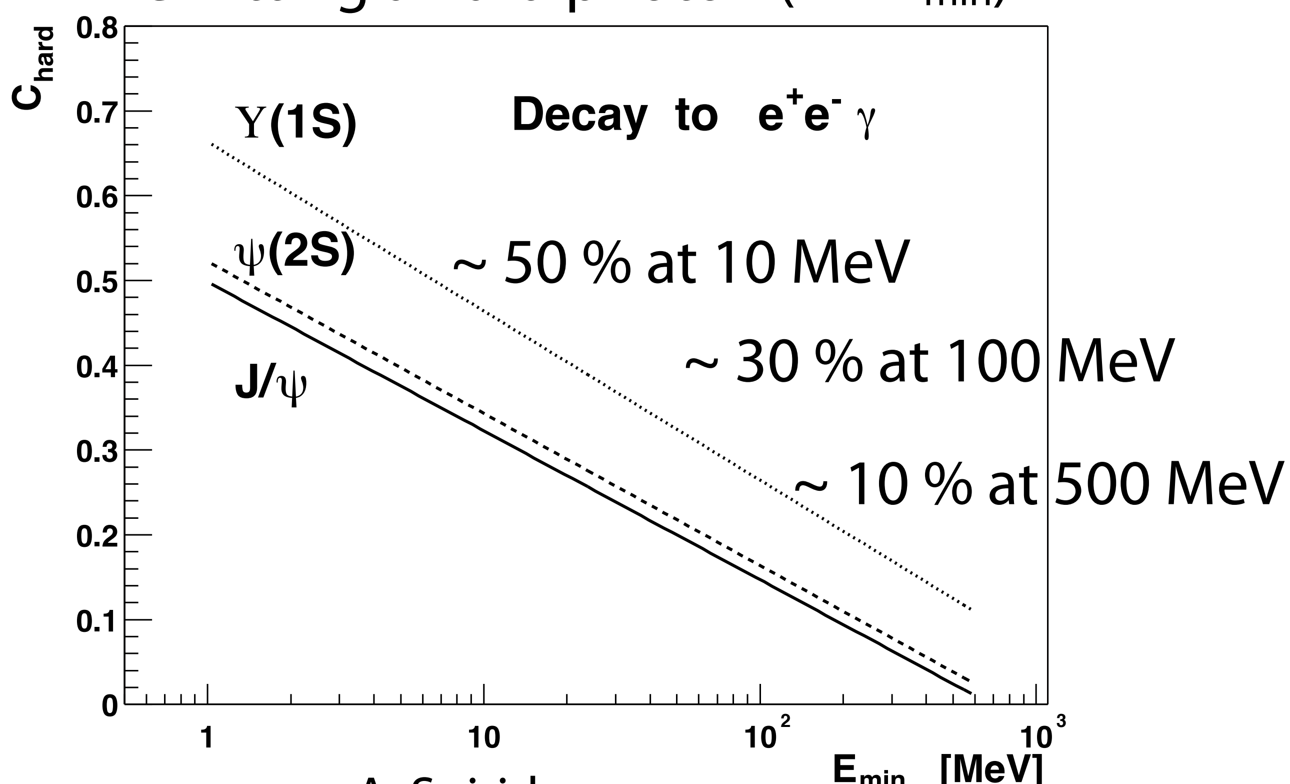


Material budget for Υ measurements

There is a concern that the silicon tracker in front of outer tracker can degrade mass resolution of Υ due to radiative energy loss in the silicon tracker.

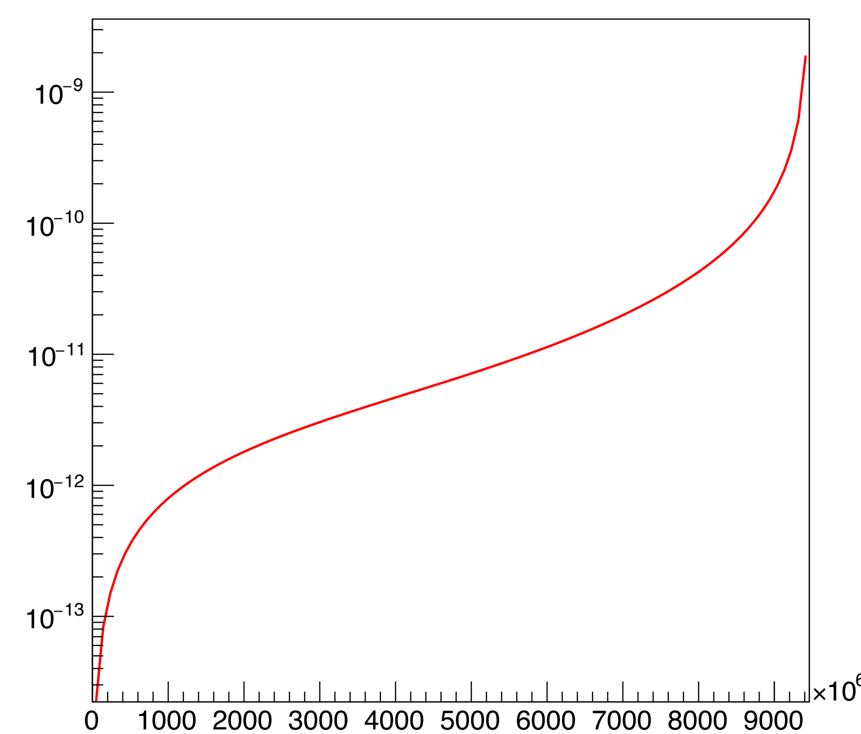
However, there is intrinsic radiative tail caused by $\Upsilon \rightarrow e^+e^-\gamma$ (Internal Bremsstrahlung). This effect must be considered when we evaluate the effect of material in the internal tracking detector.

Fraction of the internal Bremsstrahlung emitting a hard photon ($E > E_{min}$)



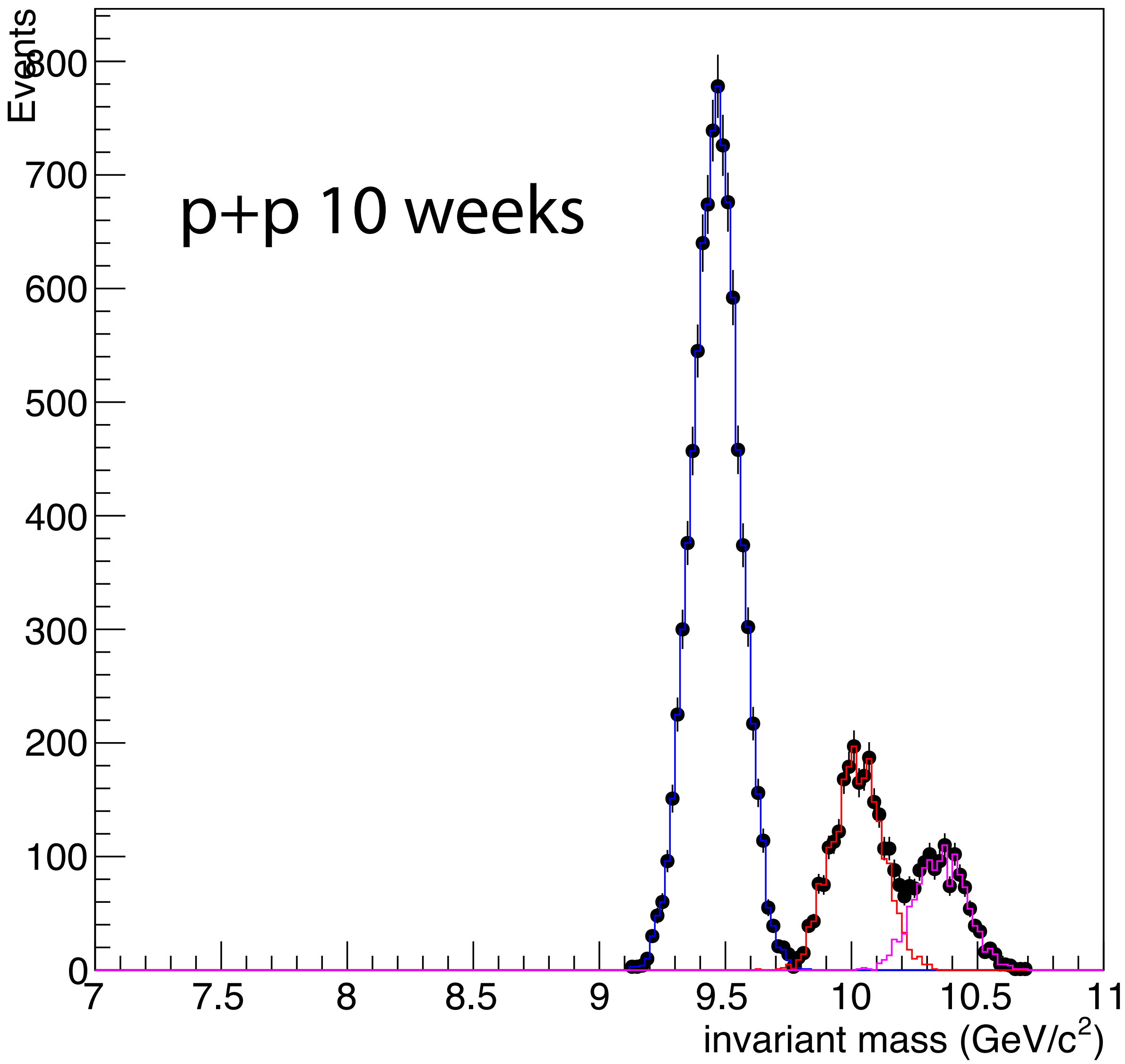
A. Spiridonov
hep-ex/0510076

Dielectron mass (Υ(1S) decay)

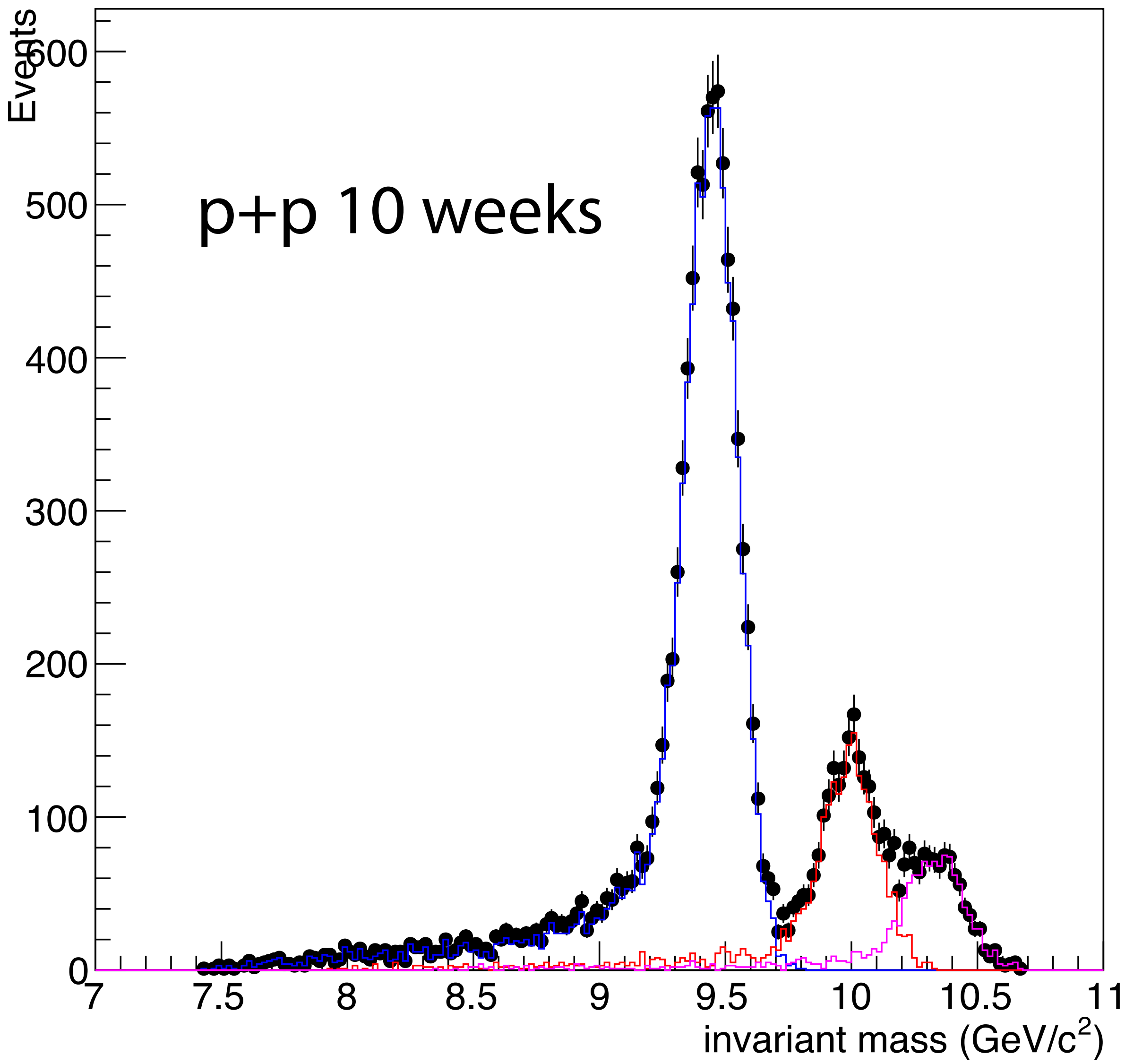


Internal Bremsstrahlung in Y decay

1 % resolution
+ no internal Bremsstrahlung



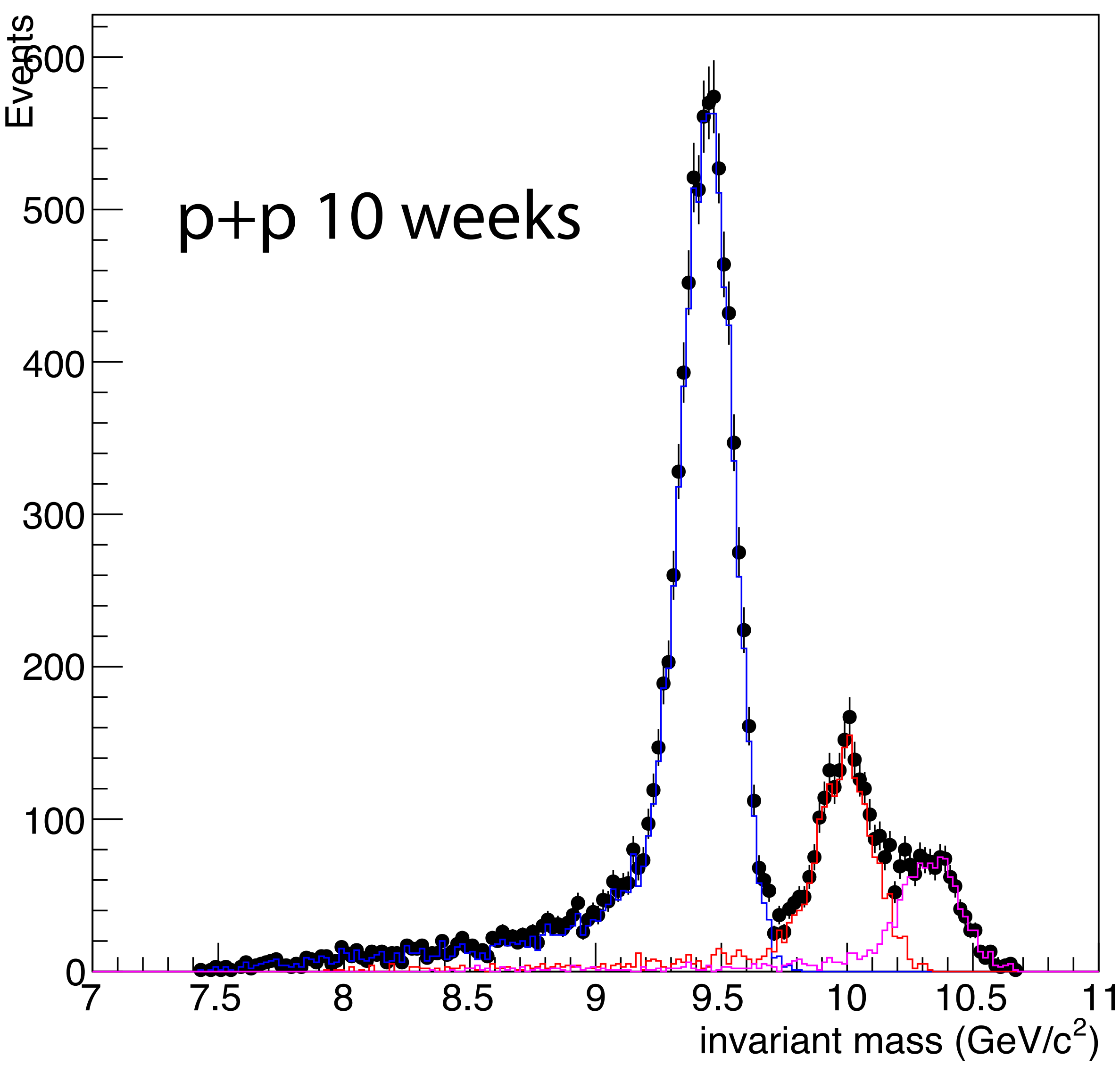
1 % resolution
+ internal Bremsstrahlung



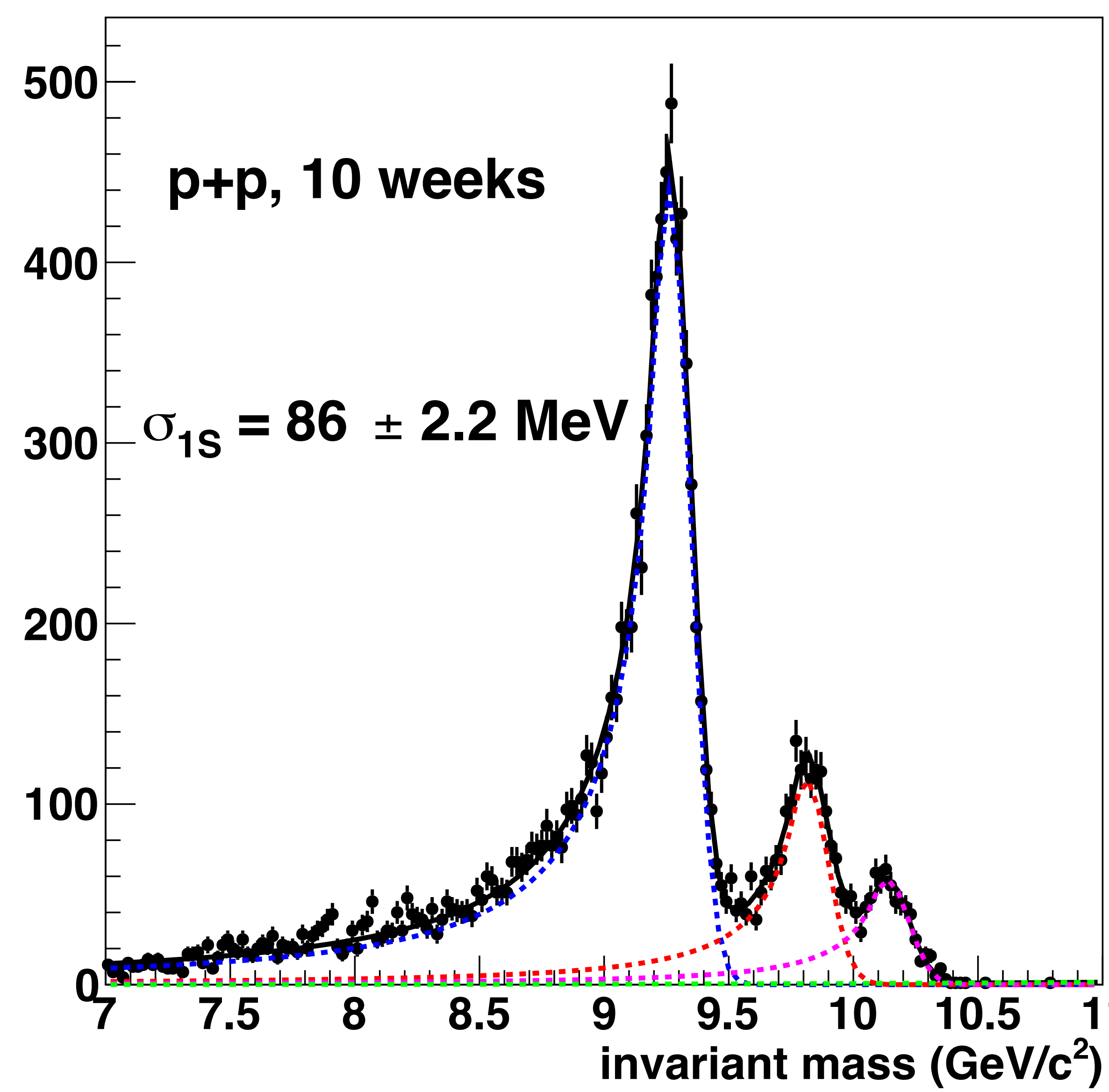
There is a substantial radiative tail due to internal Bremsstrahlung even with a massless detector. Internal bremsstrahlung is unavoidable.

Internal Bremsstrahlung in Υ decay

1 % resolution
+ internal Bremsstrahlung



pCDR G4 detector (6.8 % X_0)
+ internal Bremsstrahlung



Detector material corresponding to 6.8 % X_0 has no significant effect to Υ(2S)/Υ(3S) separation.

Scenarios

- Detector configuration depends on available funding resources.
- ***Minimal scenario:*** compact intermediate tracker (< 1M USD)
  - need outer tracker for high-momentum resolution
  - purpose of this tracker is only to connect outer tracks to the pixel detector
  - at least two layers of si-strip (three layers for redundancy) to determine the position and the momentum of a track.
- ***More funding:*** silicon layers at larger radius (~ 5M USD)
  - better standalone momentum-resolution
  - most outer layer at R ~ 50 cm can achieve sufficient momentum resolution to separate the three Υ states.

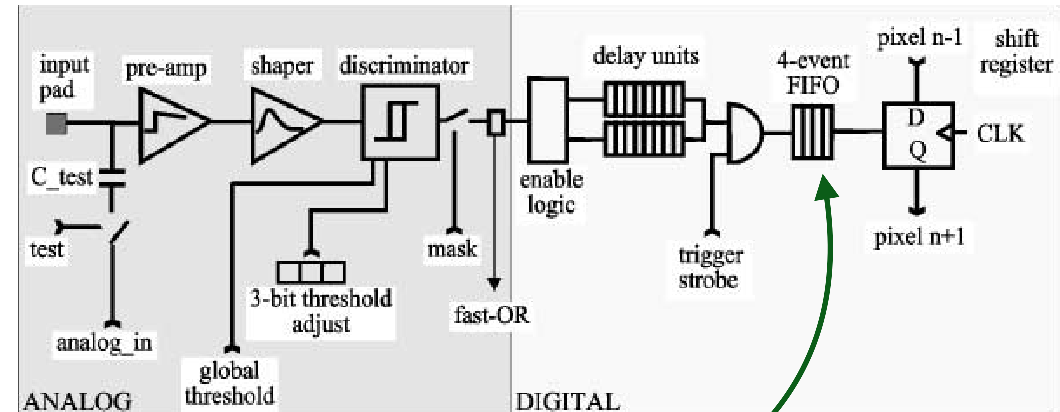
Funding requests in Japan

- We will apply funding requests for JSPS in October, 2016; both 500M JPY (~ 5M USD) and 200M JPY (~ 2M USD) grant.
- 200M JPY can make intermediate tracking system (R < 20cm).
- 500M JPY can make large tracking system (R < 50cm).

VTX pixel reconfiguration

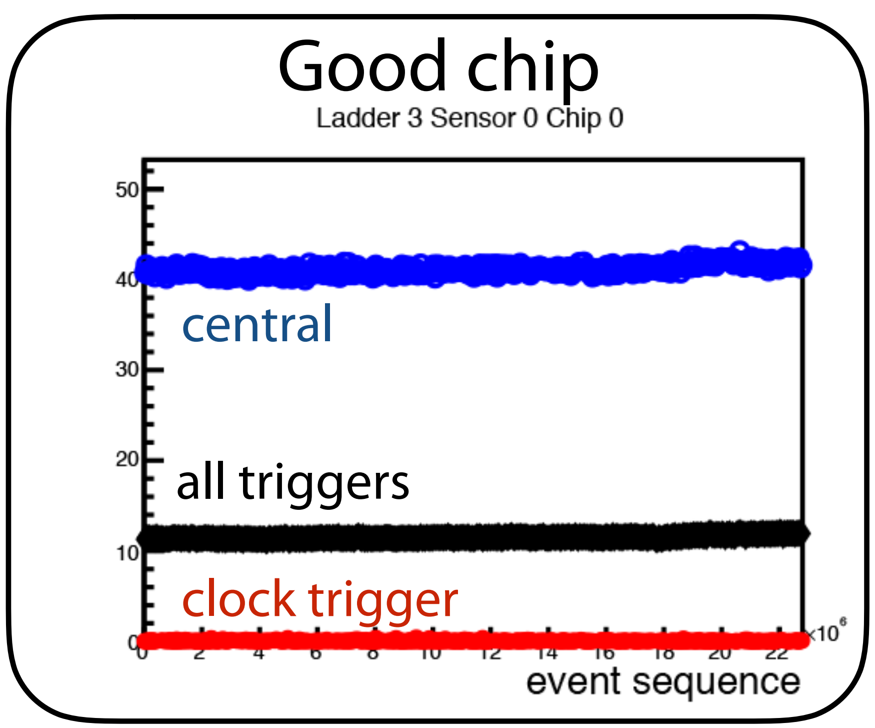
Status of VTX pixel

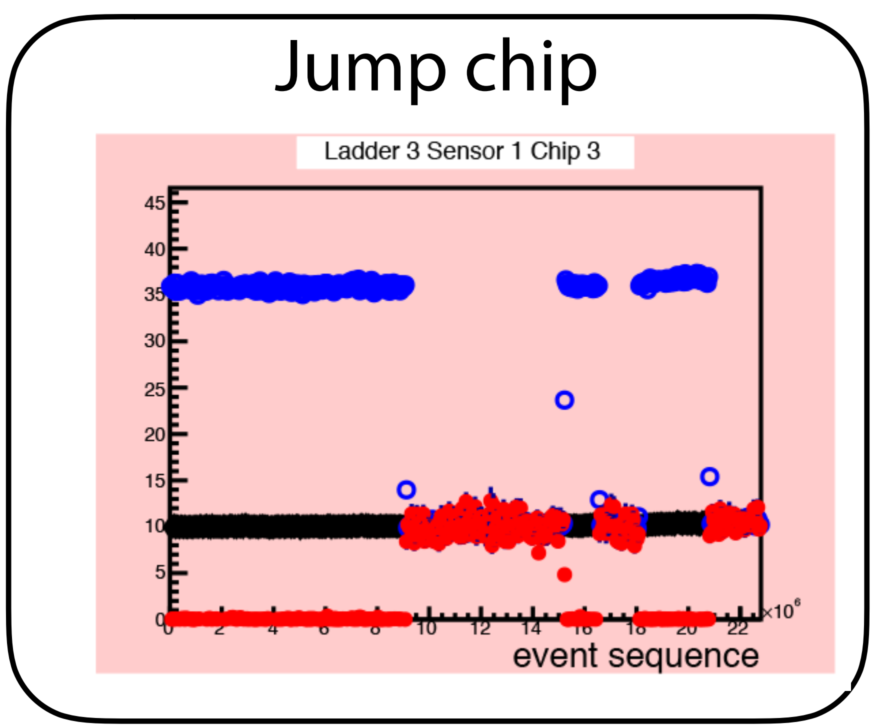
- As you may know and be worried, VTX pixel has had a “event misalignment” problem.
  Run12-15: 10-20%
  Run16: more serious than former runs.



- Event misalignment has been caused by the four-events buffer (FIFO) in the ALICE1LHCb readout chip.

- But we don’t yet fully understand why the four-events buffer is faulty working. We have already contacted ALICE people.



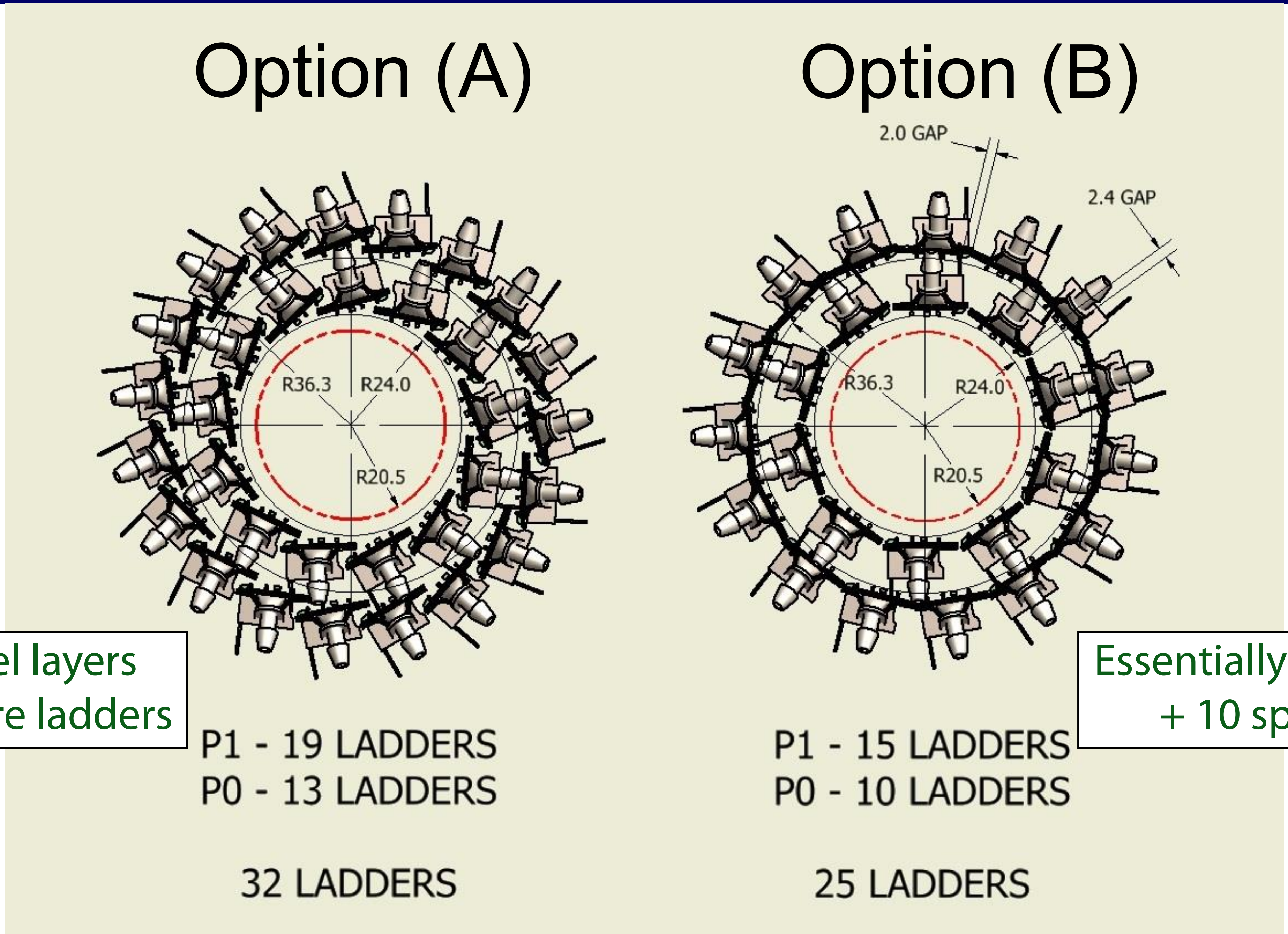


Jump chip:
FIFO pointer faulty points a wrong buffer occasionally, and then a different even is sent to a downstream fronted board.

(courtesy of K. Hill)

Integration plans

Other Options: of P0 and P1 Barrels Integration sPHENIX



Two pixel layers
+ few spare ladders

Essentially one pixel layer
+ 10 spare ladders

Conclusion: P0 and P1 configuration depends on how many good ladders we have (See next slide).

Inventory

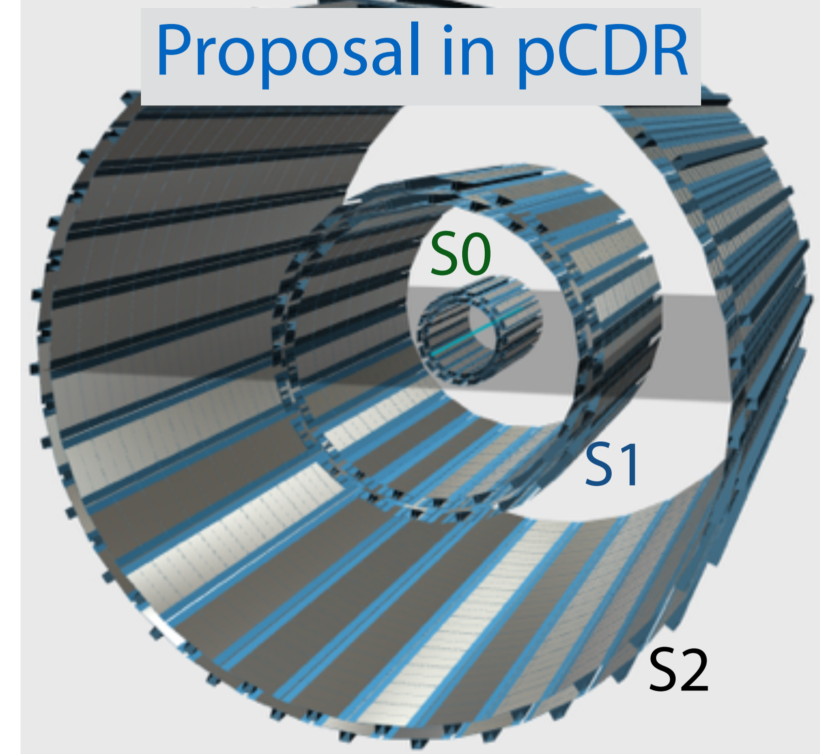
	Ladder ID	Working Pixels (%)	Location		Ladder ID	Working Pixels (%)	Location
01	L43 (new)	94.4	BNL	21	L14 (used)	79.8	BNL
02	L47 (new)	94.4	BNL	22	L16 (used)	79.7	BNL
03	L41 (new)	94.3	RIKEN	23	L35 (used)	79.4	BNL
04	L46 (new)	94.1	RIKEN	24	L5 (used)	78.6	BNL
05	L44 (new)	94.0	RIKEN	25	L12 (used)	77.4	BNL
06	L45 (new)	93.2	RIKEN	26	L25 (used)	75.3	BNL
07	L24 (used)	93.2	BNL	27	L6 (used)	72.9	BNL
08	L39 (used)	94.9	BNL	28	L34 (used)	72.0	BNL
09	L8 (used)	90.1	BNL	29	L11 (used)	71.8	BNL
10	L17 (used)	89.3	BNL	30	L15 (used)	70.7	BNL
11	L26 (used)	87.4	BNL	31	L18 (used)	69.3	BNL
12	L19 (used)	84.7	BNL	32	L10 (used)	66.1	BNL
13	L36 (used)	84.6	BNL	33	L32 (used)	61.7	BNL
14	L33 (used)	83.4	BNL	34	L27 (used)	44.7	BNL
15	L23 (used)	83.4	BNL	35	L20 (used)	32.6	BNL
16	L31 (used)	83.3	BNL	36	L30 (used)	0.0[a]	BNL
17	L22 (used)	82.9	BNL				
18	L9 (used)	80.8	BNL				
19	L21 (used)	80.4	BNL				
20	L13 (used)	80.4	BNL				

Table 11: Available silicon pixel ladders and location

[a]this is caused by failure in wire bonding and can be repaired after Run-16

(http://www.phenix.bnl.gov/phenix/WWW/publish/rnouicer/VTX/2016_VTX/Technical_Note_Silicon_Pixels_Tracker.pdf)

Si-strip detector R&D



Current status

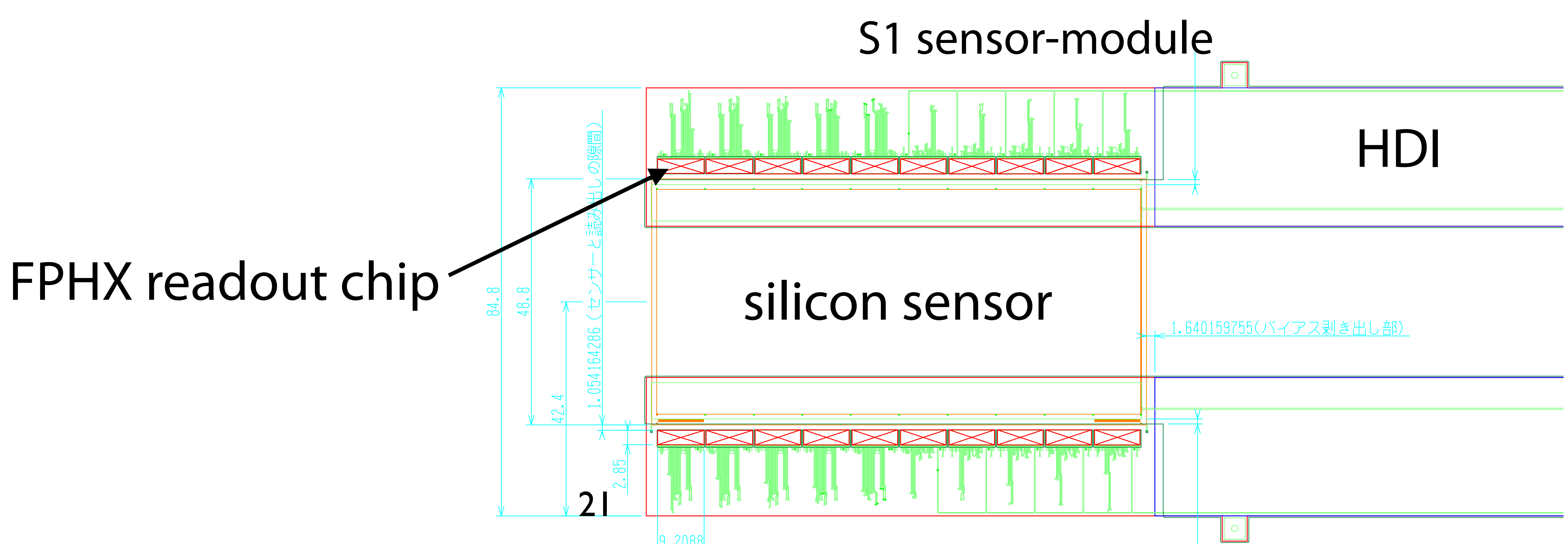
S1 station R&D work in progress.

- HDI (flexible printed circuit) design completed.
- Manufacturing of HDI starts soon.
- Silicon sensors are in our hands and will be shipped to BNL.
- Sensor-module will be tested at BNL using the FVTX test bench.
  - preparation for the readout system is ongoing.
  - air cooling test

S0 station R&D starts in this year.

- based on the common technic as the S1 station.

Continue R&D work in JFY2016 within RIKEN operation money.

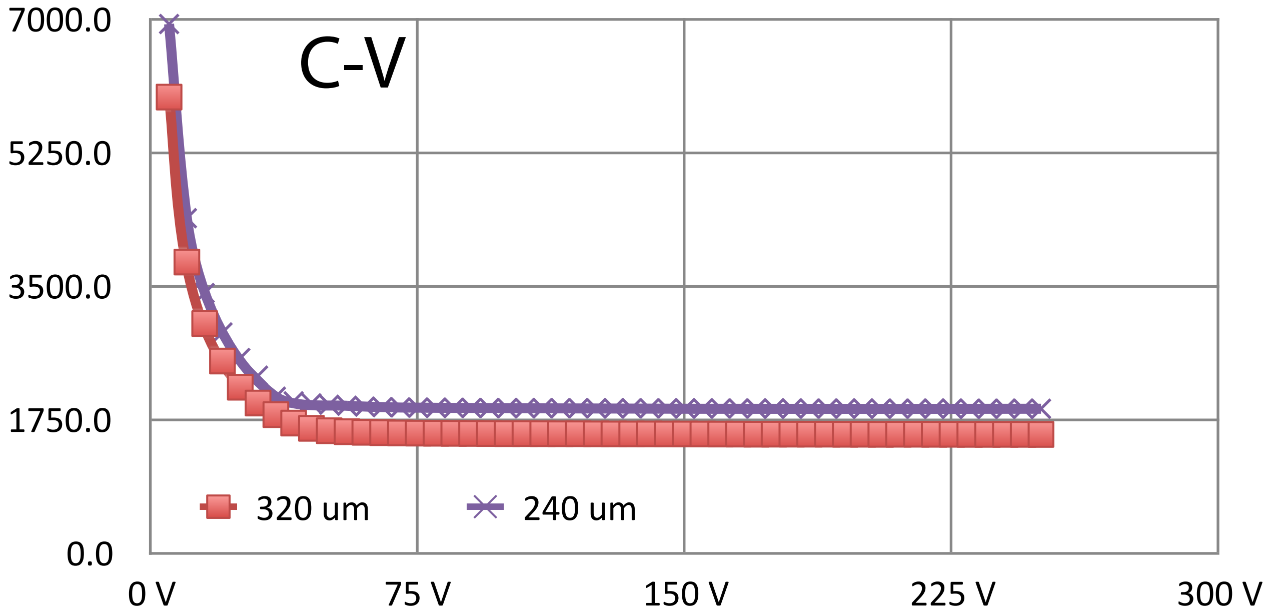


2016 R & D Schedule

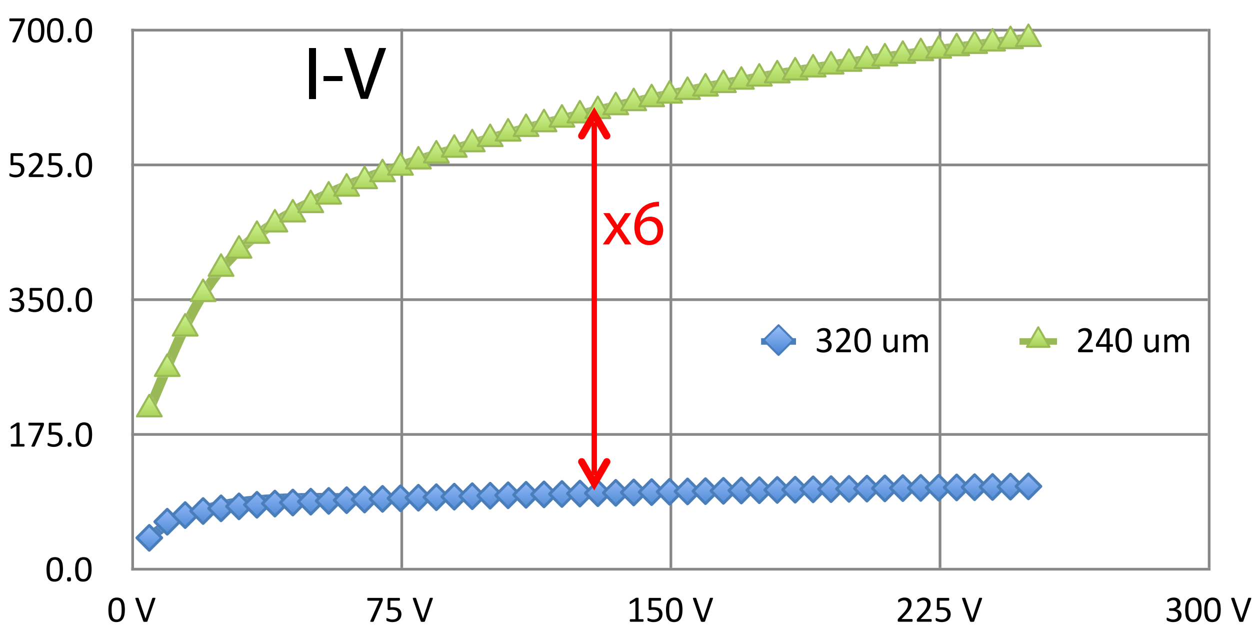
2016 Month	4	5	6	7	8	9	10	11	12	1	2	3	4	Location	Design
s1 Layer															Production
Silicon Sensor-I														Japan	Test
HDI prototype-I														Japan	
Silicon Module-I														BNL (+RIKEN)	
Silicon Sensor-II														Japan	
HDI prototype-II														Japan	
Silicon Module-II														BNL (+RIKEN)	
HDI prototype-III														Japan	
Silicon Module-III														Japan	
s0 Layer															
Silicon Sensor-I														Japan	
HDI prototype-I														Japan	
Silicon Module-I														BNL (+RIKEN)	

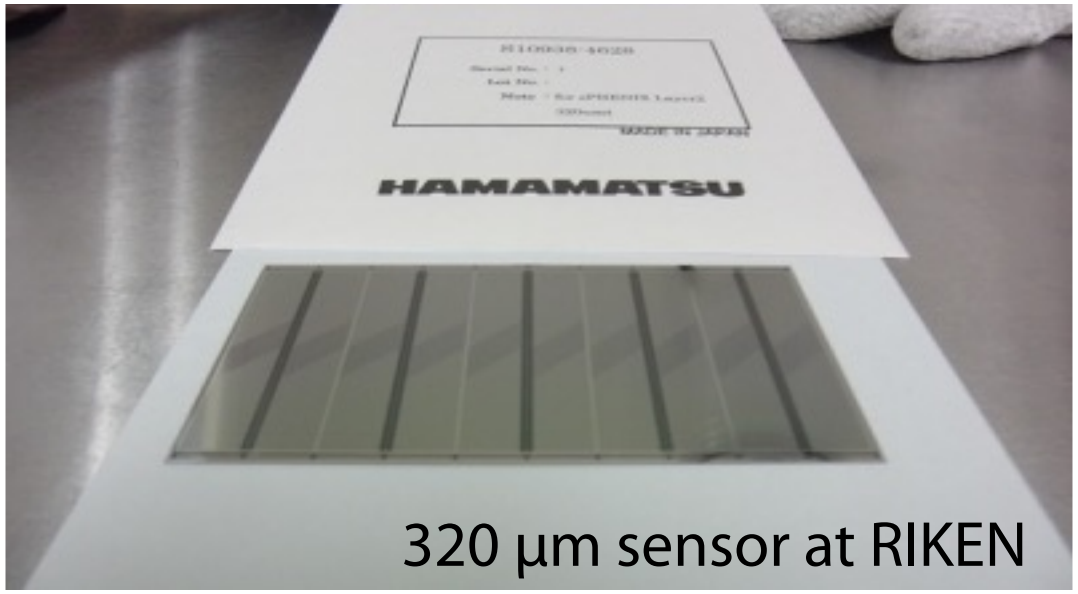
Today

Silicon sensors



Thickness	320 mm	240 mm
Full Depletion Voltage [V]	45	< 45





320 μm sensor at RIKEN

Thickness	200 μm	240 μm	320 μm
X0	0.21%	0.26%	0.34%
Dark current / 320μm	similar with 240μm	x6	x1
Price	> 0.5k USD?	0.4k USD	0.3k USD

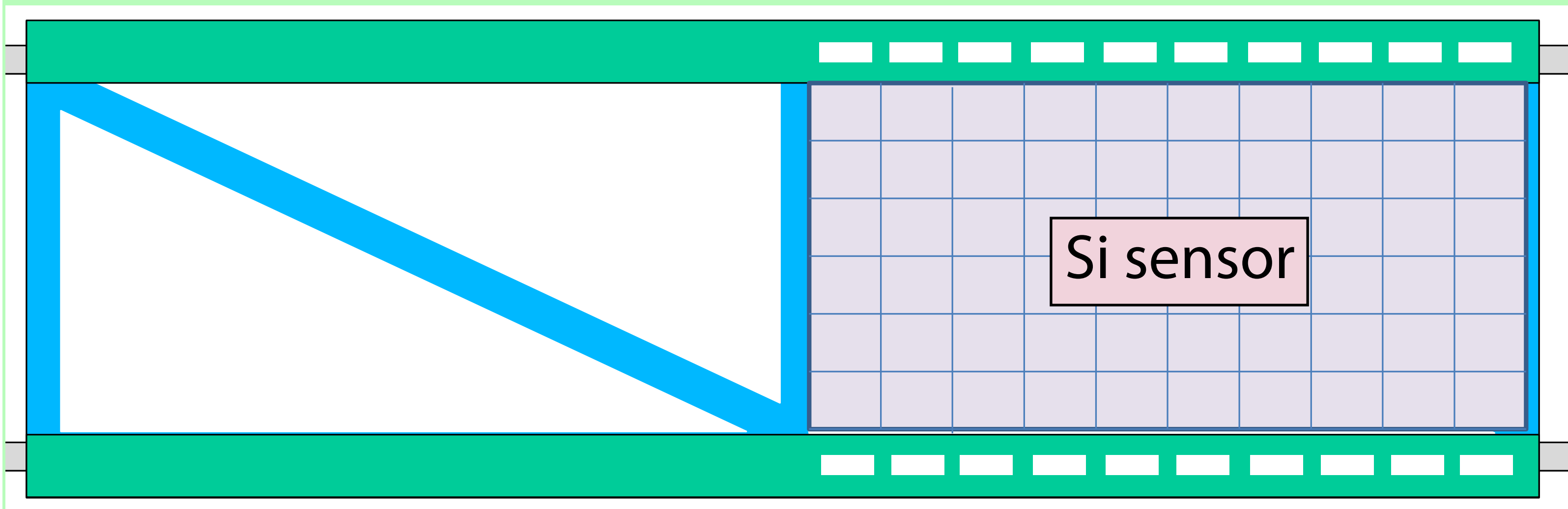
Silicon sensors for the strip layers

- Two thicknesses, 240 μm and 320 μm.
- 240 μm sensor is made by grinding 320 μm one.
- Hamamatsu says 200 μm is possible.

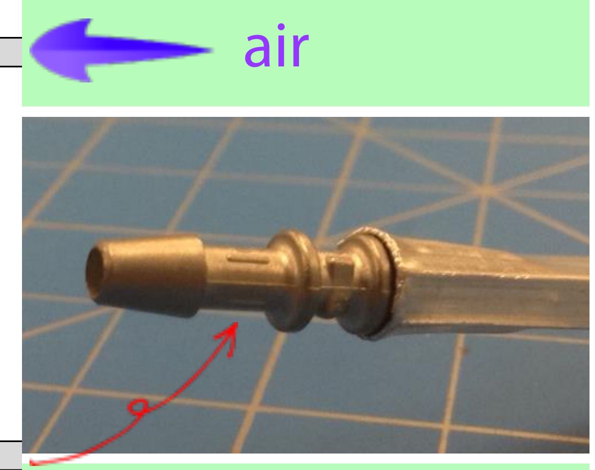
  → compromise with increasing dark current.

Is air cooling really feasible?

We will soon start a air cooling test at BNL with silicon sensors, HDI, and FPHX.

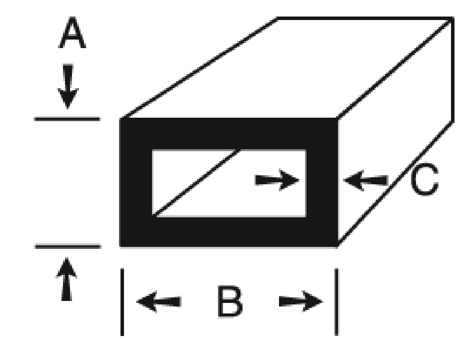


HDI FPHX (x10)

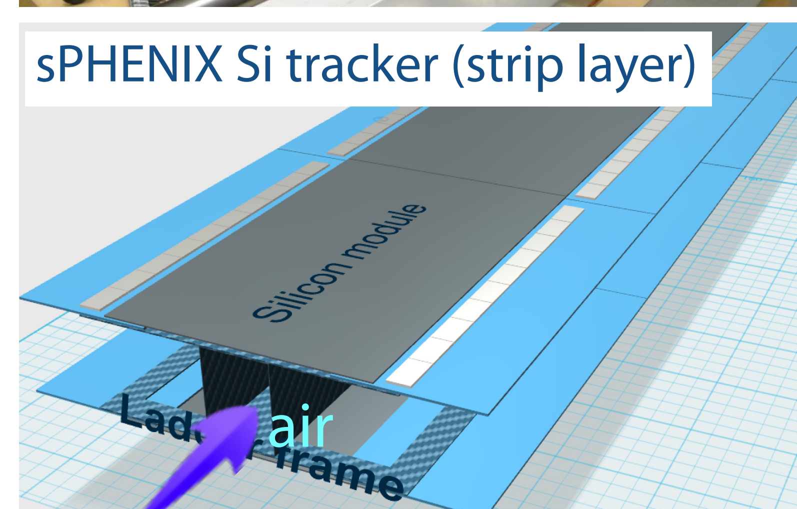


(courtesy of R. Nouicer)

Rectangular Aluminum Tube
3003 Aluminum
(A) = 0.125" = 3.175 mm
(B) = 0.250" = 6.35 mm
(C) = 0.014" = 0.355 mm



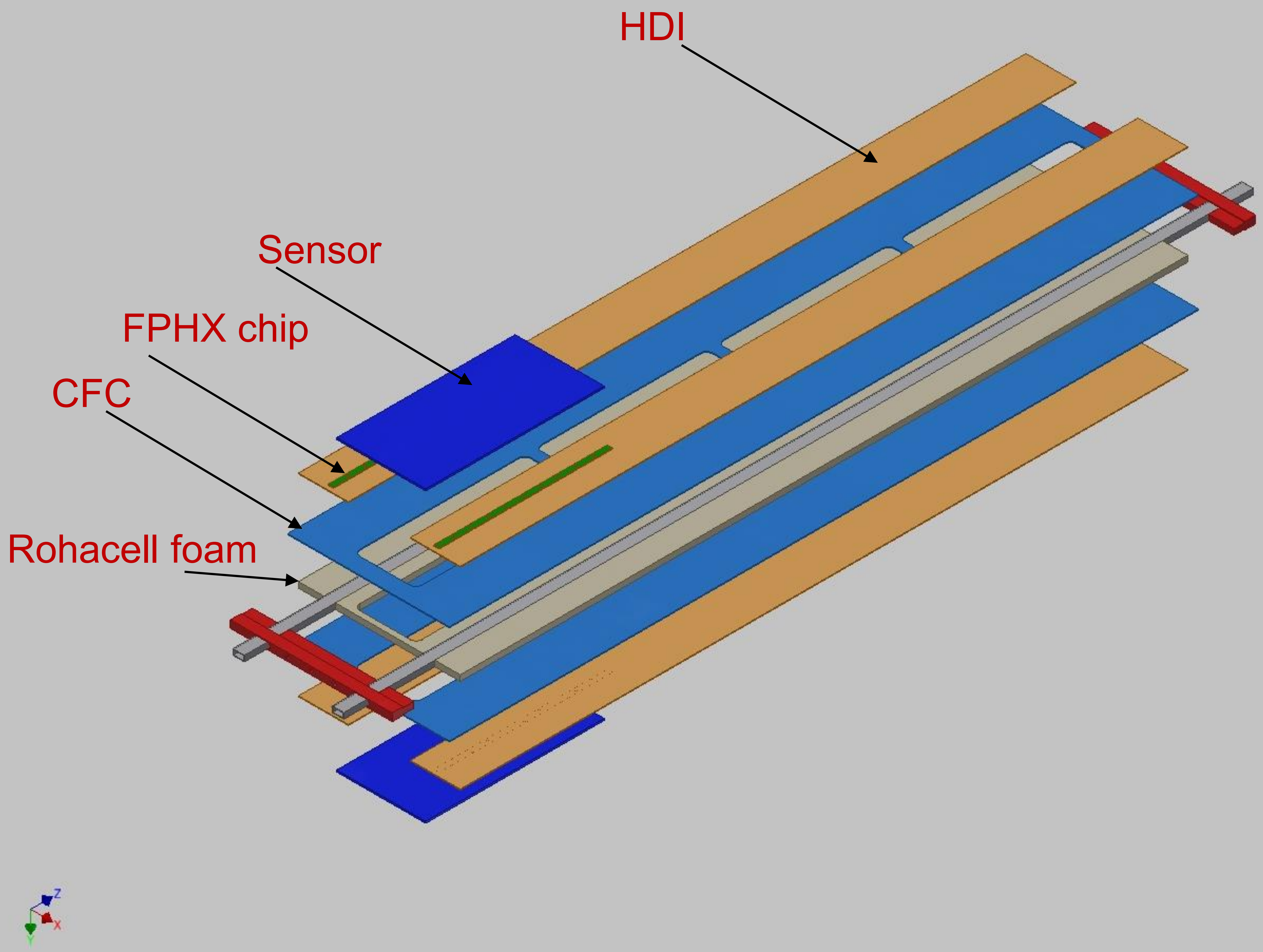
1. Temporal cooling tubes by Al
   (finally carbon tubes with 230 μm thick CFRP will be used.)
2. Air blowing with 0℃ and 10 m/s into Al tubes.
3. Temperature monitoring by diode and/or thermography camera.



Key issues

- Air cooling at STAR HFT-PXL (170 mW/cm^2, air by 0℃ and 10 m/s), but PHENIX FVTX with the FPHX chip uses coolant.
- Si tracker has 280 mW/cm^2.
- Vibration by air flow?
- Test results will be reflected to the 2nd stage design.

Stave Design for Silicon Prototype

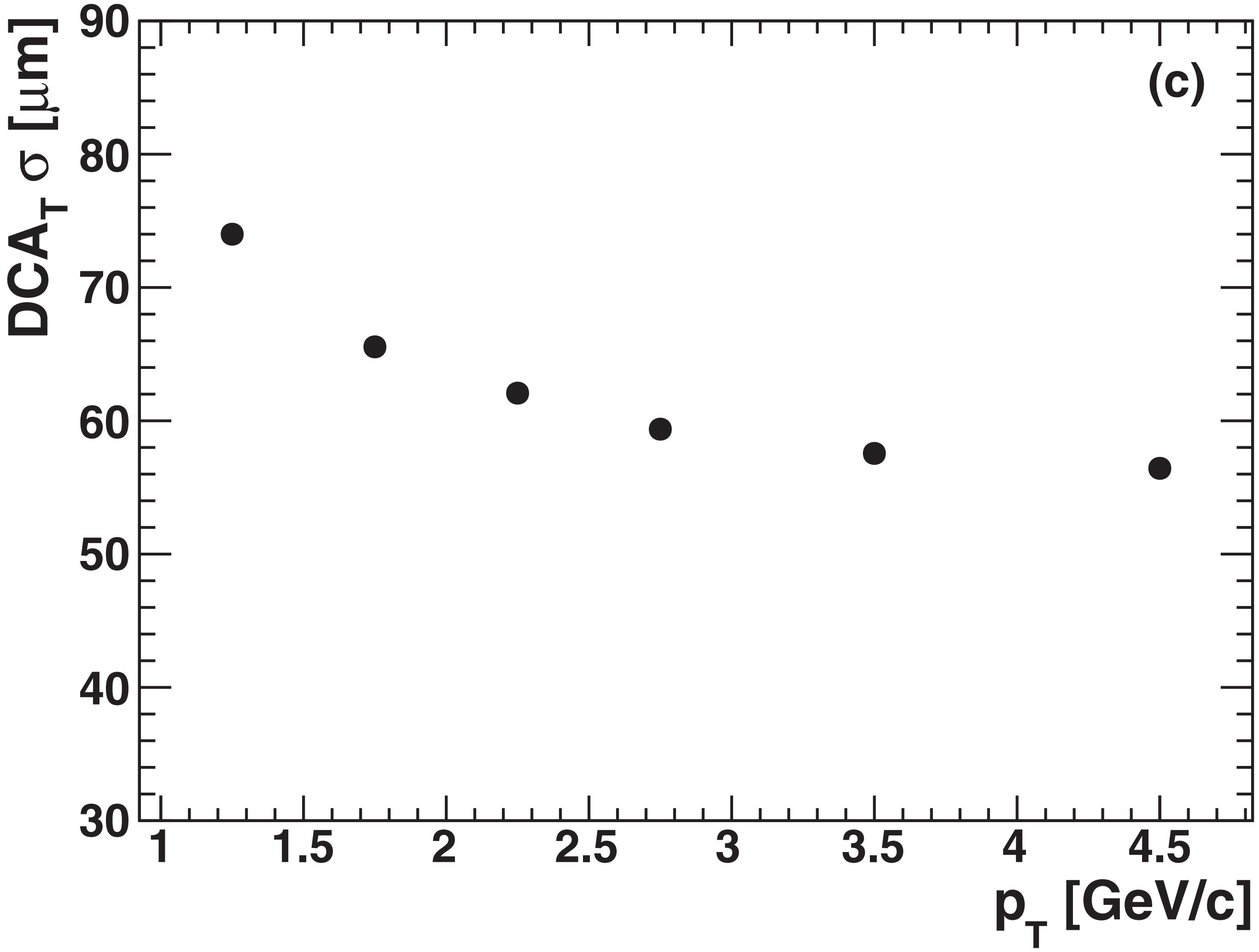


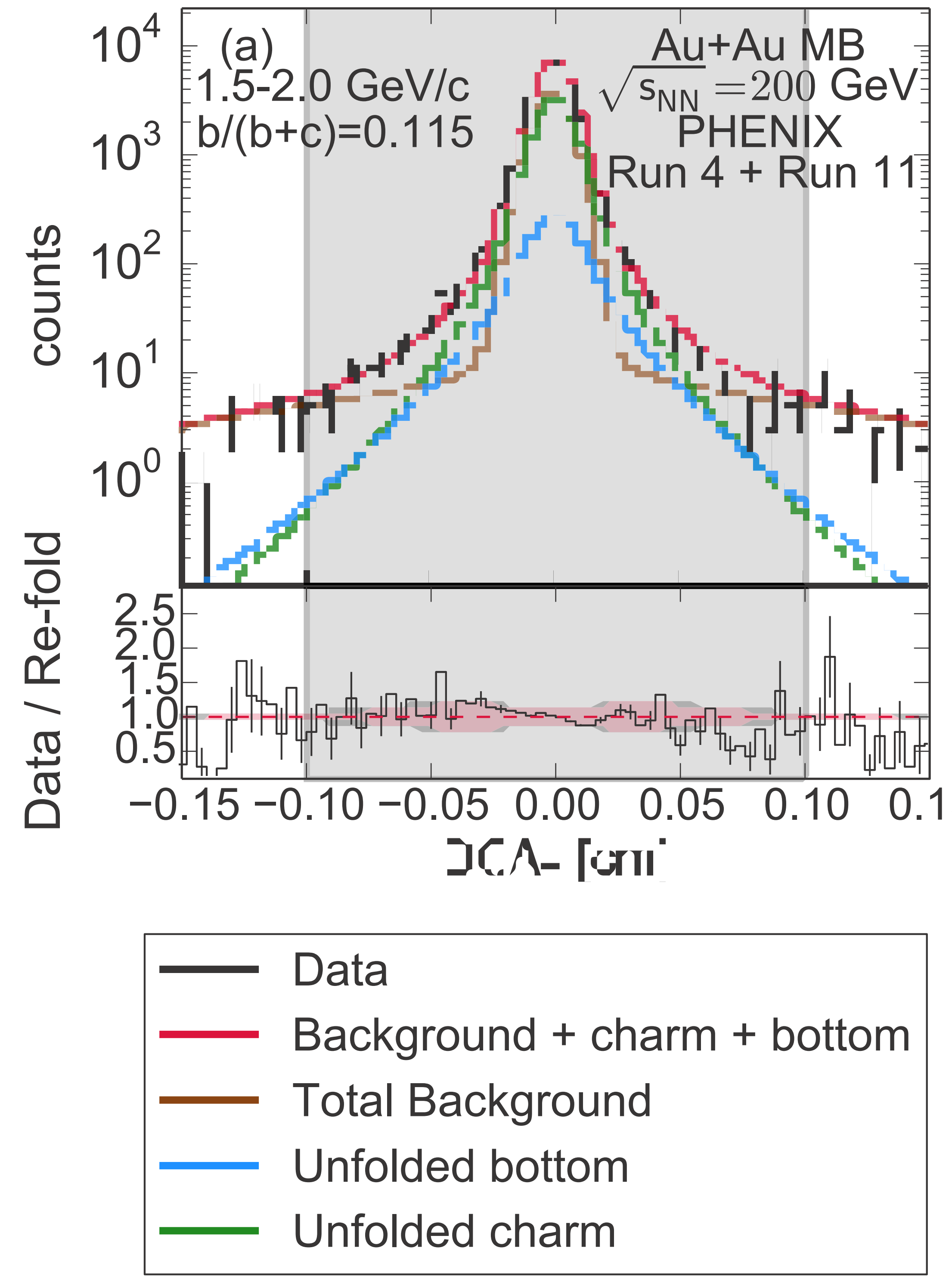
Summary

- We need 1 pixel layer + 3 or more tracking layers.
- VTX pixel should be maintained as is to be ready for re-use.
- Si-strip tracker meets physics-driven requirements and is also cost efficient.
- Integration work and R&D are work in progress.

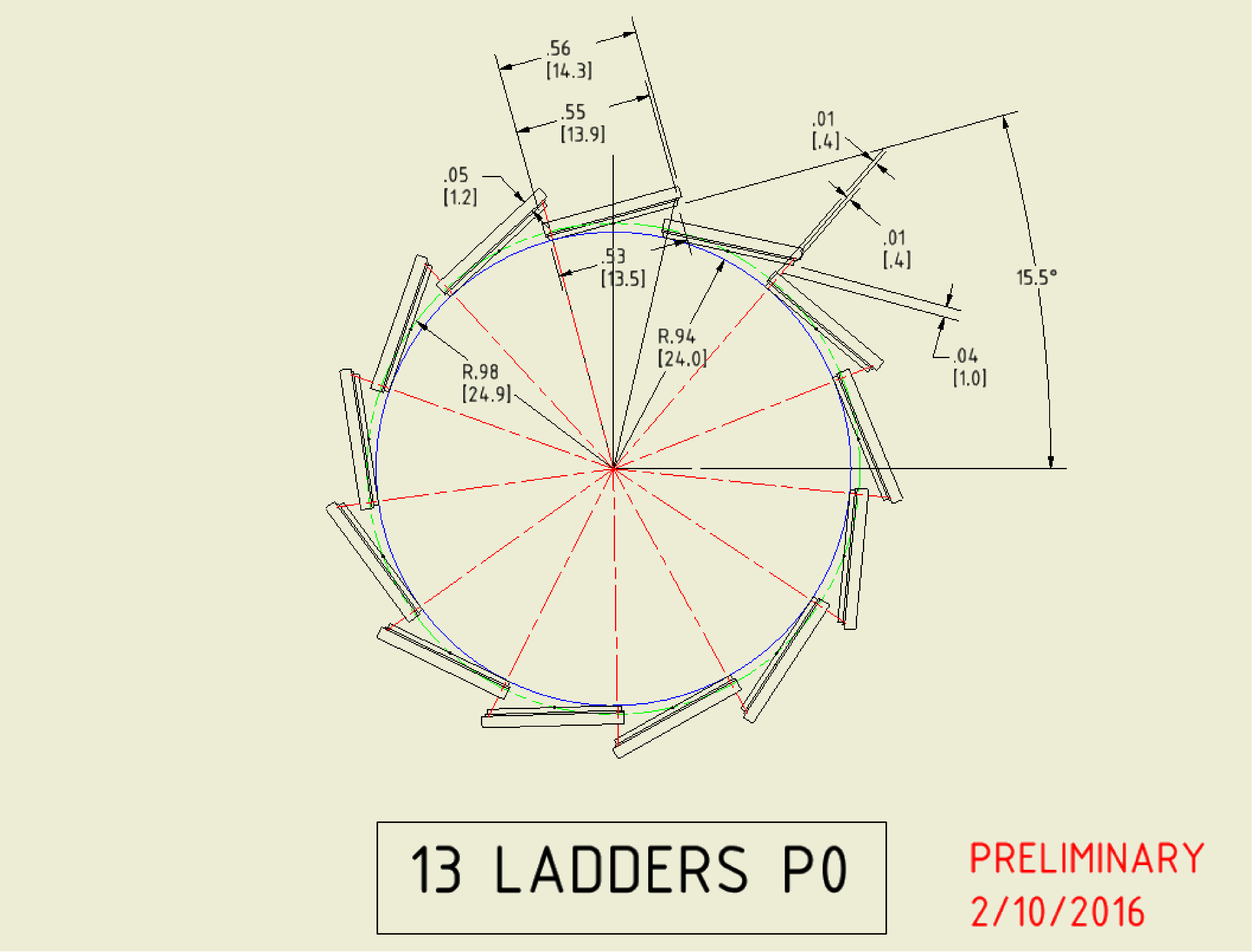
Backup

DCA distribution





➢ How many ladders are needed for P0 to have full coverage in sPHENIX?



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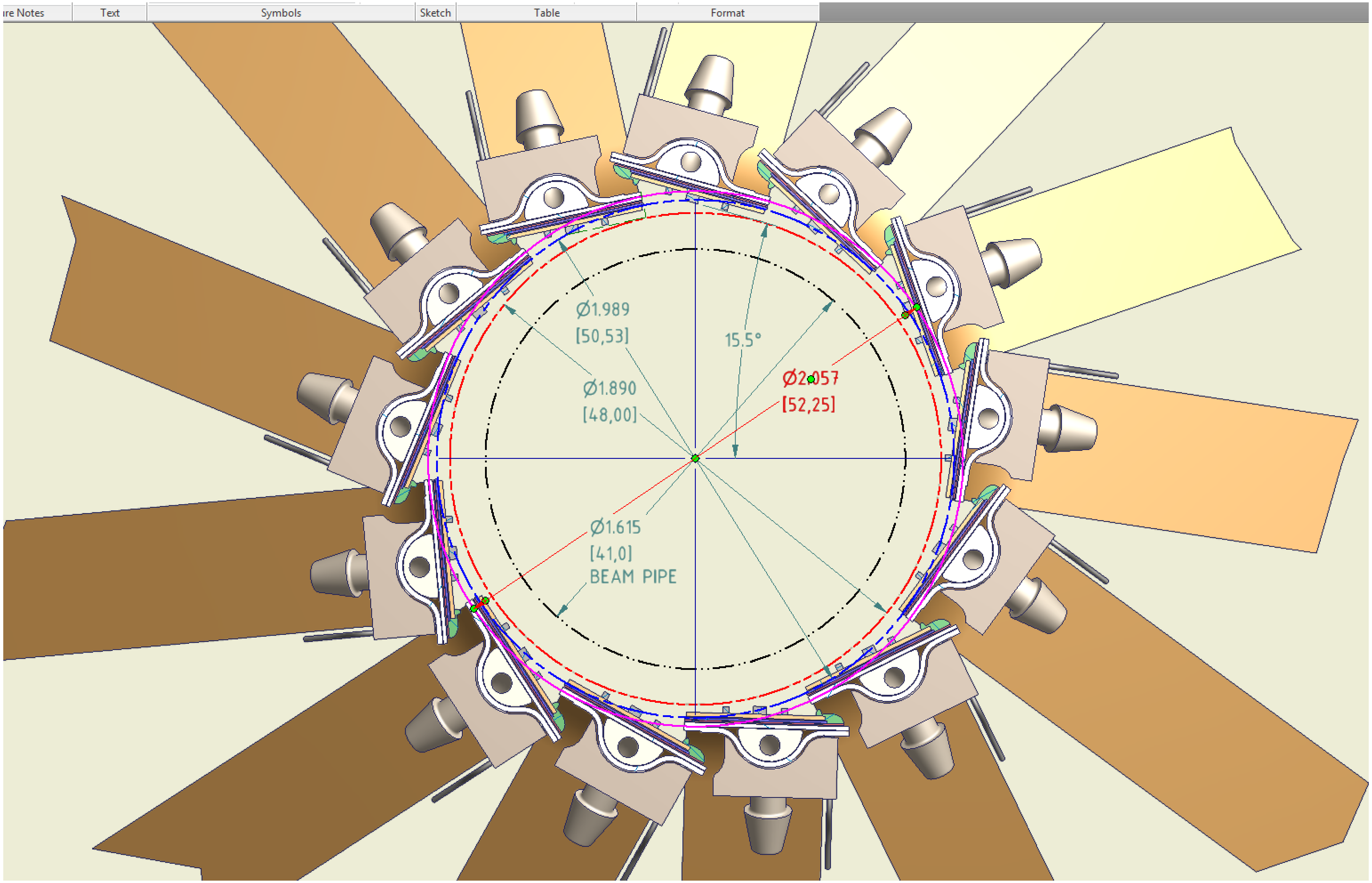
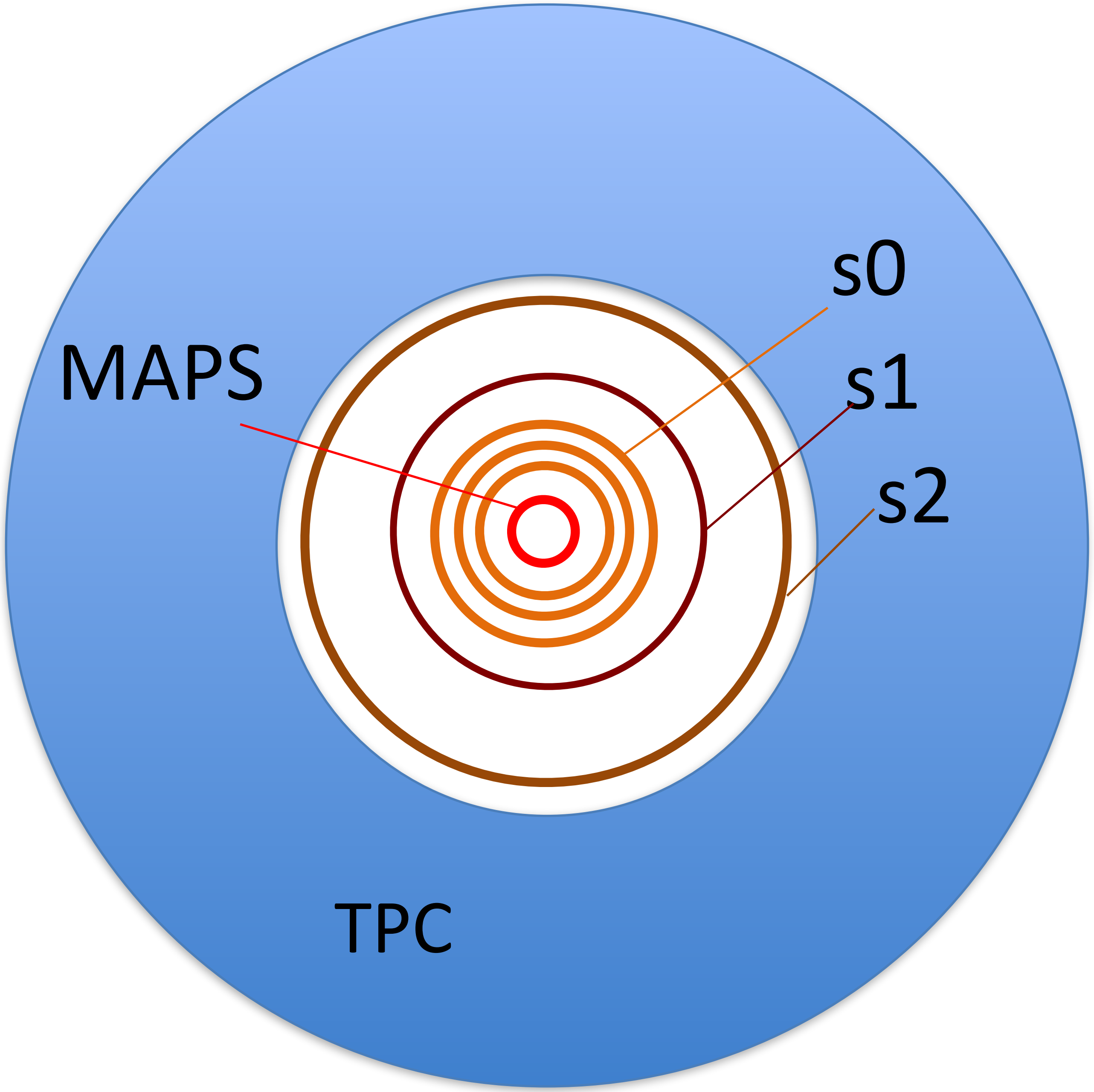


Silicon Sensor Concept



- Rather compact design to fit between MAPS and TPC
- Interconnect between MAPS hits and TPC tracks